Amendments to the Specification:

Please replace paragraph [0006] with the following replacement paragraph:

[0006] It is also known to implement loops in phases. For example, U. S. Patent No. 6,445,231 ~~Application No.~~ [[_____,]] ~~filed~~ [[_____,]] ~~(Micron No. 98-0788)~~ entitled Digital Dual-Loop DLL Design Using Coarse and Fine Loops illustrates a circuit in which the delay line is comprised of both a coarse loop and a fine loop. The coarse loop is designed to produce an output signal having a phase variation from an input signal within a ~~course~~ coarse delay stage while the fine loop is designed to produce an output signal having a phase deviation from the input signal which is substantially smaller than the deviation of the coarse loop. The coarse loop is designed to bring the output signal to a near phase lock condition, or phase delayed condition, while the fine loop is designed to achieve a locked condition. Thus, a dual-loop (coarse and fine loops) all digital PLL or DLL can provide a wide lock range while at the same time still providing a tight lock within reasonable time parameters.